16. (Amended) The method as claimed in claim 15, wherein the step of calibrating the output driver comprises deriving the second output from a signal provided directly by the output driver.

17. (Amended) The method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a resistive divider.

18. (Amended) The method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a transconductance stage.

19. (Amended) The method as claimed in claim 16, wherein the step of deriving the second output comprises applying the signal to a switched capacitor circuit.

20. (Amended) The method as claimed in claim 15, wherein the first current control signal is applied under user control.

Please add new claims 21-23 as follows:

21. (New) The method of claim 1, wherein the current mode driver is a mutli-PAM signal generator coupled to a bus.

22. (New) The method of claim 21, wherein the sensing, adjusting and setting steps occur during a power-up sequence for the mutli-PAM signal generator.

23. (New) The method of claim 21, wherein the adjusting and setting steps occur in response to a triggering event after power-up.

REMARKS

In the Office Action of June 18, 2002, the Examiner objected to claims 2-10, 12-14 and 16-20 because of informalities in the claim language. In addition, the Examiner rejected claims 1-4, 7, 9, 11, 12, 14-16 and 20 under 35 U.S.C. § 102(e) as being anticipated by Sandhu et al. The Examiner rejected claims 5 and 6 under 35 U.S.C. § 103 as being unpatentable over Sandhu et al. in view of Gillig. Claim 8 was rejected under 35 U.S.C. § 103 as being unpatentable over Sandhu et al.

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in view of Georgiou et al. The Examiner rejected claims 10, 18 and 19 under 35 U.S.C. § 103 as being unpatentable over Sandhu et al. in view of Nguyen. Claim 13 was rejected under 35 U.S.C. § 103 as being unpatentable over Sandhu et al. Finally, the Examiner rejected claim 17 under 35 U.S.C. § 103 as being unpatentable over Sandhu et al. in view of Fattaruso. Applicants respectfully traverse the rejections and request reconsideration.

I. Claim Objections

The Examiner objected to claims 2-10, 12-14 and 16-20 because the preamble of each of these dependent claims begins with "A method," rather than "The method." Claims 2-10, 12-14 and 16-20 have been amended to recite "The method," as requested by the Examiner. Applicants therefore submit that claims 2-19, 12-14 and 16-20 are no longer objectionable.

II. Section 102 Rejection

The Examiner rejected claims 1-4, 7, 9, 11, 12, 14-16 and 20 under 35 U.S.C. § 102(e) as being anticipated by Sandhu et al. Because Sandhu et al. fail to show every element of those claims, however, applicants traverse the rejection.

A. Sandhu et al.

Sandhu et al. show a thermal sensor 20 (Fig. 4) and describe a method of trimming the thermal sensor 20. The thermal sensor 20 many be used to monitor a substrate temperature of a microprocessor and, when the temperature exceeds a threshold, to alter an internal clock signal (CLK_INTERNAL) to reduce thermal buildup in the substrate. Col. 10, lines, 4-13; Col. 3, lines 47-67 and Col. 1, lines 59-67.

Sandhu et al. states that the thermal sensor 20 is permanently calibrated during a test mode. Col. 5, lines 35-42. The calibration routine, shown in Figure 5 of Sandhu et al., utilizes a digital interface 26 to supply two four-bit signals, 71 and 72, where each bit of the four bit signal is uniquely coupled to one current source 22 to either enable or disable the current source 22. Col. 5, lines 43-48. During calibration, the four-bit signals, 71 and 72, are changed to find the values that drive the THERMAL_TRIP signal 27 high. Col. 6, lines 40-65. The values are then used to program fuses that permanently enable/disable the current sources 22. Col. 6, lines 61-65.

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B. Sandhu et al. Fail to Show the Claimed Invention

As an initial matter, Sandhu et al. fail to describe a method of "improving resolution of a current mode driver," as recited in claims 1 and 15, or a method of "improving resolution of the output driver," as recited in claim 11. Contrary to the suggestions in the June 18th Office Action (see page 1, paragraph 5), neither the thermal sensor 20, shown in Fig. 4 of Sandhu et al., nor the current sources 22 therein, constitute any type of current mode driver or output driver. As described in the present application, for example at pages 11-12, drivers generate signals that are transmitted over a bus. The circuitry shown by Sandhu et al. in Fig. 4 merely serves to generate the THERMAL_TRIP signal 27, which is substantially different than bus signaling.

In addition, Sandhu et al. fail to show the steps recited in the claimed methods. For example, Sandhu et al. fail to show the step of "adjusting a full scale current of a DAC in accordance with the sensing step," as recited in claim 1. In this regard, Sandhu et al. fail to even mention a full scale current, much less any capability of adjusting a full scale current. In the thermal sensor 20 shown by Sandhu et al., the current sources 22 are selectively enabled in an open-ended manner by digital interface 26 to adjust a reference voltage, VREF. No mention of a full scale current or its adjustment is made by Sandhu et al.

Nor do Sandhu et al. show the step of "setting a current control signal based on an output of the DAC, the current control signal being applied to the current mode driver," as recited in claim 1. As noted above, Sandhu et al. fail to show a current mode driver. As such, Sandhu et al. also clearly fail to show a current control signal applied to a current mode driver.

Similar deficiencies arise in comparing Sandhu et al. to the method claimed in claim 11. In particular, Sandhu et al. fail to show "applying the current control signal to cause the output driver to sink a full scale current," as recited in claim 11. Nor do Sandhu et al. show "generating a full scale adjustment signal at the PVT detector." Nor do Sandhu et al. show "applying the full scale current adjustment signal to alter the full scale current of the output driver," as recited in claim 11.

Likewise, Sandhu et al. fail to show the method of claim 15. Specifically, Sandhu et al. fails to show "applying the first output as a gate voltage to control a full scale current of an output driver," as recited in claim 15. Nor do Sandhu et al. show "calibrating the output driver by comparing a second output, which is provided by the output driver, with a reference." Sandhu et al.

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also fail to show "augmenting the first current control signal when the second output (from the output driver) differs from the reference.

Because Sandhu et al. fail to show at least the foregoing elements of claims 1, 11 and 15, those claims are not anticipated by Sandhu et al. The allowance of dependent claims 2-10, 12-14 and 16-20 will follow directly from the allowance of claims 1, 11 and 15.

III. Section 103 Rejections

The Examiner rejected claims 5, 6, 8, 10, 13 and 17-19 under 35 U.S.C. § 103(a) as being unpatentable over various combinations of references, in which Sandhu et al. is the primary reference. The failures of Sandhu et al. to show the claimed methods of improving the resolution of an output driver are described above. Likewise, none of the secondary references, namely Gillig, Georgiou et al., Nguyen et al. and Fattaruso et al., provide any showing or suggestion for improving the resolution of an output driver as claimed. All of the references, including Sandhu et al., miss the mark by failing to show or suggest the claimed methods for improving the resolution of an output driver.

In addition, the Examiner's combination of these references in support of the obviousness rejections is improper. It is insufficient, as suggested by the Examiner, that the references are "from a similar problem solving area." Rather, the references themselves must suggest the propriety of the combination. *In re Dembiczak*, 175 F.3d 994 (Fed. Cir. 1999); *In re Lee*, 27 F.3d 1338 (Fed. Cir. 2002). For example, with respect to Gillig and Sandhu et al., there is no suggestion in Sandhu et al. that the temperature sensor 20 would be useful in a piezoelectric frequency oscillator, like that shown in Gillig. Nor does Gillig include any suggestion that its locked loop circuits would be useful in a temperature sensor, like the sensor 20 of Sandhu et al. Applicants submit that it is only with improper hindsight and knowledge of the present invention that one might consider such a combination.

Furthermore, even if the references are combined, they fail to render obvious the claimed invention. Claims 5 and 6, for example, recite the use of a phase-locked loop and a delay-locked loop, respectively, in sensing a process condition for improving resolution of a current mode driver. Neither Sandhu et al. nor Gilling show or suggest such methods. In fact, the locked loop circuits of Gillig are independent of the temperature sensor 226 and seemingly play no role whatsoever in sensing temperature, as recited in claims 5 and 6. The combination of Sandhu et al. and Gillig

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therefore fails to render the subject matter of claims 5 and 6 obvious.

Likewise claim 8 recites a sensing step that comprises applying a pulse in parallel to a delay line and plurality of latches, coupling the delay line to the latches, and decoding a latch output. Neither Sandhu et al. nor Georgiou et al. show or suggest the recited structure. Nor does either reference even suggest using such structure to sense a PVT condition. In Georgiou et al., the circuit of Fig. 3 merely applies a delay value 135 to delay the dispatch of instructions to a functional unit. Applicants therefore submit that the subject mater of claim 8 is patentable over the combination of Sandhu et al. in view of Georgiou et al.

Claims 10, 18 and 19 are rejected as being unpatentable over Sandhu et al. in view of Nguyen. Nguyen shows a temperature monitor that uses a switched capacitor, band gap voltage reference. An input capacitor, Cin, shown in Fig. 3, is used to sample the constituent voltages of the band gap reference, which are then summed by the integrator 36. Contrary to the Examiner's suggestion, the input capacitor, Cin, does not represent an AC parameter. Rather, the circuit appears to produce a DC weighted summation of the constituent DC voltages. Moreover, even if properly combined, Sandhu et al. and Nguyen fail to show or suggest the calibrating step, which relates to calibrating an output driver.

Finally, the Examiner rejected claim 17 as being unpatentable over Sandhu et al. in view of Fattaruso et al. Fattaruso et al. describe the use of a low impedance shunt to adjust the value of a resistor string. Fattaruso et al., however, whether taken alone or in combination with Sandhu et al., fail to show or suggest calibrating an output driver by applying a signal from the output driver to a resistive divider. Thus, the combination of Sandhu et al. in view of Fattaruso et al. fails to render obvious the subject matter of claim 17.

New Claims

New claims 21-23, which depend ultimately from claim 1, have been added. No new matter has been added.

In light of the foregoing remarks, applicants respectfully submit that the present application is in condition for allowance and such action is respectfully requested. The applicants invited the Examiner to call the undersigned at (312) 913-0001 with any questions or comments.

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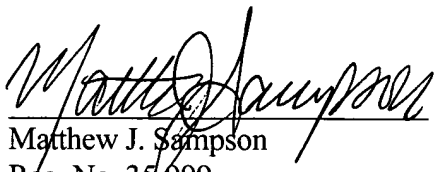
Respectfully submitted,

Date: September 18, 2002

By: 

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